ΣΧΕΔΙΑΣΗ ΨΗΦΙΑΚΩΝ ΣΥΣΤΗΜΑΤΩΝ

# ΑΣΚΗΣΗ 2

ΑΠΟΚΩΔΙΚΟΠΟΙΗΤΗΣ 2 ΣΕ 4

library ieee;

use ieee.std\_logic\_1164.all;

entity decoder2to4 is

begin

port(

a: in STD\_LOGIC\_VECTOR(1 downto 0);

b: in STD\_lOGIC\_VECTOR(3 downto 0)

);

end decoder2to4;

architecture arc of decoder2to4 is

begin

process(a)

begin

case a is

when "00" => b <= “0001”;when "01"=> b <= “0010”;when "10"=> b <= “0100”;when "11"=> b <= “1000”;

end case;

end process;

end arc;

ΠΟΛΥΠΛΕΚΤΗΣ 2 ΣΕ 1 ΜΕ ΕΠΙΛΟΓΗ

library ieee;

use ieee.std\_logic\_1164.all;

entity decoder2to4 is

begin

port(

a: in STD\_LOGIC\_VECTOR(1 downto 0);

b: in STD\_lOGIC\_VECTOR(3 downto 0)

);

end decoder2to4;

architecture arc of decoder2to4 is

begin

process(a)

begin

case a is

when "00" => b <= “0001”;when "01"=> b <= “0010”;when "10"=> b <= “0100”;when "11"=> b <= “1000”;

end case;

end process;

end arc;

ΑΠΟΚΩΔΙΚΟΠΟΙΗΤΗΣ 2 ΣΕ 4

library ieee;

use ieee.std\_logic\_1164.all;

entity decoder2to4 is

begin

port(

a: in STD\_LOGIC\_VECTOR(1 downto 0);

b: in STD\_lOGIC\_VECTOR(3 downto 0)

);

end decoder2to4;

architecture arc of decoder2to4 is

begin

process(a)

begin

case a is

when "00" => b <= “0001”;when "01"=> b <= “0010”;when "10"=> b <= “0100”;when "11"=> b <= “1000”;

end case;

end process;

end arc;

ΤΡΙΠΛΟΣ ΠΟΛΥΠΛΕΚΤΗΣ (3 ΒΙΤ) 2 ΣΕ 1

entity mux\_3bit\_2to1 is

port(

s : in STD\_LOGIC;

a , b: in STD\_LOGIC\_VECTOR(2 DOWNTO 0);

d : out STD\_LOGIC\_VECTOR(2 DOWNTO 0)

);

END mux\_3bit\_2to1;

architecture arc of mux\_3bit\_2to1 is

begin

d <= a when s = ‘0’ else

b when s=’1’ else

null;

end arc;